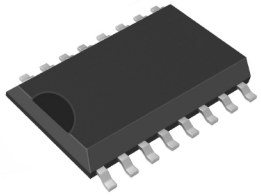
REAL TIME CLOCK IC（Built-in Crystal Oscillator）

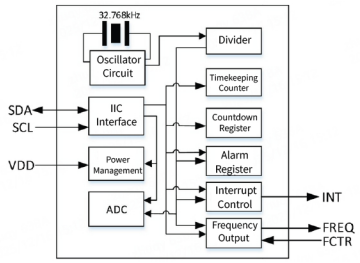
High-precision

ST8825

- Low power consumption: 0.6μA typical (VDD =3.0V, Ta=25°C).
- Operating voltage: 2.5V~5.5V; Timekeeping: 1.5V～5.5V.
- Operating temperature: -40°C~+105°C.
- ROHS Recognized
- Standard IIC bus interface, maximum speed 400KHz (4.5V~5.5V).
- Chip pin ESD>4KV
- CMOS Process
- Package Form:SOP14(198mil).



Block diagram



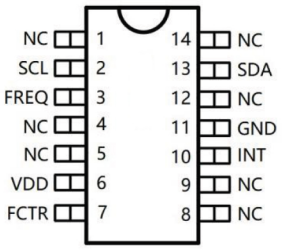
Overview

- Internal 70-byte general-purpose SRAM
- high-precision timing within A wide temperature range: 25°C<1ppm(Class A),-40°C to +85°C<5ppm,+86°C to +105°C<10ppm .
- Built-in IIC bus 0.5 seconds automatic reset function
- Built-in 1/1024 second register
- Built-in communication verification function
- Built-in clock data write-protection function

Pin Function

Name	Function	Feature
SCL	Serial clock input pin. Signal processing occurs on the rising/falling edges of SCL. Special attention should be paid to the rise/fall times of the SCL signal, and the datas heet must be strictly followed. To reduce the SCL rise time, the MCU pin connected to SCL can be configured as CMOS output; do not set it as open-drain output.	CMOS Input
FREQ	Frequency output pin controlled by FCTR. See FCTR pin description for details.	CMOS Output
VDD	Positive power supply pin	—
FCTR	Enables/disables FREQ pin output: FCTR=0, FREQ output disabled; FCTR=1, FREQ out put enabled.	CMOS Input
INT	Interrupt output pin. Its operating mode is set via control registers.	N-channel open-drain output
GND	Ground (GND)	—
SDA	Serial data input/output pin, this pin is usually pulled up to VDD with a resistor, and connected to other devices with open drain or open collector outputs via wire-AND logic.	N-channel open-drain output / CMOS Input
NC	Not connected internally within the chip	—

Terminal connection



Characteristics

- DC characteristics

Symbol	Parameter	Condition	Min Value	Typical Value	Max Value	Unit
V_{DD}	Main Power Supply		2.5		5.5	V
V_{keep}	Keep-Alive Voltage		1.5		5.5	V
I_{DD1}	Main Power Supply Current	$V_{DD}=5V$		0.6	1.2	μA
		$V_{DD}=3V$		0.5	1.0	μA
I_{DD2}	Power Supply Current during IIC Communication	$V_{DD}=5V$		40	120	μA
I_{L1}	Input Leakage Current of SCL			100		nA
I_{L0}	Input/Output Leakage Current of SDA			100		nA
V_{OL}	Low-Level Output Voltage of INT / SDA	$V_{DD}=5$ $I_{OL}=0.5mA$	0.1	0.2	0.3	V
V_{DDR}	Rate of Rise of VDD during Power-On Reset		0.1		1	V/ms
V_{temp}	Temperature Compensation Threshold Voltage			2.4		V

- Frequency Error & Temperature Relationship Curve