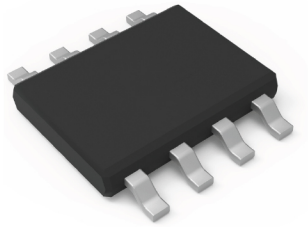
REAL TIME CLOCK IC（Built-in Crystal Oscillator）

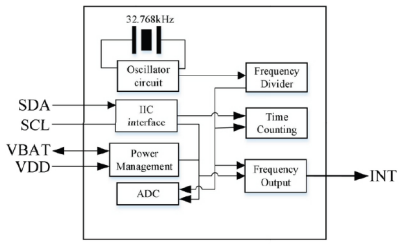
High-precision

ST8938

- Low power consumption: 0.6μA typical (Ta=25°C).
- Operating voltage: 1.8V~5.5V; Timekeeping voltage: 1.5~5.5V.
- Operating temperature: -40°C~+105°C.
- Accuracy at room temperature is <±5ppm.
- Standard IIC bus interface mode, maximum speed 400kHz.
- Chip pin ESD>4KV
- Pass 4 kV EFT Interference Test
- CMOS Process
- Package Form:SOP8(150mil)



Block diagram



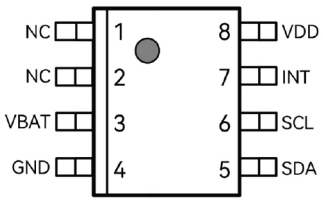
Overview

- Built-in 1/1024 second register
- Built-in IIC bus 0.5 seconds auto reset function
- Built-in temperature register
- Built-in Communication Verification Function
- Built-in 70-Byte General-Purpose SRAM Registers
- Built-in clock data write-protection function
- Built-in 8-Byte ID

Pin Function

Name	function	Features
VBAT	Backup battery input pin, built-in voltage regulator and charging current selectable charging circuit.	1.5V to 5.5V, should be connected to GND when not in use
GND	Negative power (GND)	2.5V~5.5V
SDA	Serial data input/output pin, this pin is usually pulled up to VDD with a resistor, and connected to other devices with open drain or open collector outputs via wire-AND logic.	N-Channel Open Drain Output/CMOS Input
SCL	Serial Clock Input pin. Since the signal is processed on the rising/falling edge of the SCL, special attention should be paid to the rising/falling rise/lowering time of the SCL signal, and the instructions should be strictly adhered to. In order to reduce the SCL rising edge time, the port where the MCU is connected to SCL can be set to CMOS output, do not set it to open-drain output.	CMOS input
INT	Alarm interrupt output pin	N-Channel Open Drain Output
VDD	Positive power pin	

Terminal connection



DC Characteristics

Symbol	Parameters	Condition	Min	Typical	Max	Uint
V_{DD}	Main power supply		1.8		5.5	V
V_{keep}	Timing voltage		1.5		5.5	V
V_{BAT}	Standby battery supply voltage		1.5		5.5	V
I_{DD1}	Main supply current	V_{DD}=5V		0.6	1.2	μA
		V_{DD}=3V		0.5	1.0	μA
I_{DD2}	The supply current when the IIC communicates	V_{DD}=5V		40	120	μA
I_{DD3}	Power supply current when charging is enabled	V_{DD}=5V		80		μA
I_{BAT}	Spare battery supply current	V_{BAT}=3.3V		0.6		μA
I_{LI}	The input leakage current of SCL			100		nA
I_{LO}	The input/output leakage current of the SDA			100		nA
V_{BATHYS}	Hysteresis voltage for switching between VBAT and VDD			85		mV
V_{sw}	Voltage to switch between VBAT and VDD	Ta=25℃		2.4		V
V_{OL}	INT/SDA Low Output Voltage	V_{DD}=5V I_{OL}=0.5mA	0.1	0.2	0.3	V
V_{RR}	VDD rise rate on power reset		0.1		1	V/ms